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Events and PUBLICATIONS
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VLSI Society of India has been conducting the annual VDAT or the **VLSI Design And Test Symposium**, since 1998. **VLSI Design Conference**, which has been sponsored by VSI, has grown significantly in the past 15 years, with the number of participants crossing 1000.

From the year 2005, VSI has been organizing a number of events through the year, spread across the country, to bring together the academia and the industry, that highlight the hot and emerging topics on VLSI and the related.

The proceedings of most of these workshops are available as softcopies. The VDAT Symposium proceedings are available in both hard and softcopy formats.

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	2010	SPEAKERS / INSTRUCTORS
52	Two-day workshop on Innovation through Effective Thinking March 5-6, 2010 9.30 AM - 6.00 PM; TI India, Bangalore	Kalyan Kumar Banerjee and Dr. Raghunath Govindachari (MindTree Limited)
51	Seminar on A Century of Systematic Innovation: From Edison to Lafley March 4, 2010 3.30 - 4.30 PM; TI India, Bangalore	Dr.Vinay Dabholkar
50	14th IEEE/VSI VLSI Design And Test Symposium – VDAT2010 July 7-9, 2010 – Chitkara University, Chandigarh	
49	Short course on Recent Advances in DFT and Test January 25, 2010 9.30 - 2.00 PM; TI India, Bangalore	Arvind Jain, Rajesh Tiwari, Vishwanath S, Srivaths Ravi, and Rubin Parekhji (TI India)
48	Seminar on Technology Trends and Options for High Performance CMOS FETs at the 15-nm Generation and Beyond January 5, 2010 4.00 - 5.00 PM; TI India, Bangalore	Prof. Dimitri A. Antoniadis, MIT Microsystems Technology Laboratories, Cambridge, Massachusetts
47	23rd International Conference on VLSI Design And 9th Intl Conference on Embedded Systems January 3-7, 2010 Bangalore, India	



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	2009	SPEAKERS / INSTRUCTORS
46	Conference on Communication Technologies & VLSI Design October 8-10, 2009, Vellore, Tamil Nadu In conjunction with the Silver Jubilee Celebration of VIT University, Vellore Organised by the School of Electrical Sciences, VIT University - Vellore In association with VLSI Society of India	
45	13th IEEE/ESI VLSI Design And Test Symposium – VDAT2009 July 8-10, 2009 – Wipro Campus, Bangalore	



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	2009 continued...	SPEAKERS / INSTRUCTORS
44	Economics of the Semiconductor Industry Seminar organized in association with PragaTI (TI India Technical University)	Prabir Mohanty , Texas Instruments India
43	One-day Course on Design Automation Algorithms for FPGAs 31 March 2009 - TI India Campus, Bangalore	Prof. Susmita Sur-Kolay , Senior Associate Professor, Advanced Computing and Microelectronics Unit, Indian Statistical Institute (ISI), Kolkata
42	ACM Bangalore Distinguished Speakers Program and Panel Discussion In-cooperation with IEEE-CAS Bangalore Section February 14, 2009 – Bangalore Foil of the panel discussion available under VSI Download section	Automated Design of Digital Microfluidic Lab-on-Chip Connecting Biochemistry to Information Technology and Electronic Design Automation Prof. Krishnendu Chakrabarty , Dept of ECE, Duke University Panel Discussion: Functional Diversity and More than Moore: Impact on VLSI Industry and VLSI Education Panelists: Pramod Chandra P. Bhatt , Vidha Software Solutions; Madabusi Govindarajan , IBM; Nagovolu Srinivasa Murty , NXP Semiconductors; Jagdish Rao , Texas Instruments India; C. P. Ravikumar , Texas Instruments India; and Mysore Sriram , Intel India
41	Automated Design of Digital Microfluidic Lab-on-Chip Connecting Biochemistry to Information Technology and Electronic Design Automation February 11, 2009 - TI India Campus, Bangalore Seminar organized in cooperation with PragaTI (TI India Technical University)	Prof. Krishnendu Chakrabarty , Dept of ECE, Duke University
40	Evolutionary Computation for Engineering Optimization January 16, 2009 - TI India Campus, Bangalore	Prof. C. Patvardhan , Department of EE, Dayalbagh Educational Institute, Agra
39	Common Power Format & Low Power Design January 13, 2009 - TI India Campus, Bangalore Seminar organized in cooperation with PragaTI (TI India Technical University)	Dr. Sumit DasGupta , Senior VP, Si2 (Silicon Integration Initiative)
38	Low Power Design & Verification with UPF 2.0 January 9, 2009 - TI India Campus, Bangalore Seminar organized in cooperation with PragaTI (TI India Technical University)	Stephen Bailey (Director Product Marketing, Mentor Graphics); and Gary Delp (Distinguished Engineer, LSI Corp)
37	22nd International Conference on VLSI Design And 8th Intl Conference on Embedded Systems January 5-9, 2009 New Delhi, India	



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	2008	SPEAKERS / INSTRUCTORS
36	Three-day Workshop on DSP and Embedded Systems August 18-20, 2008 – VNRVJIET Campus, Hyderabad	N. Balaji , VNRVJIET; Prohor Choudhury , Texas Instruments India; Gurjit Singh Gill , Gill Instruments; Sreeram Mohan , Cranes Software; Vivek Nittoor , ARM Embedded Technologies; Bharat Pathak , Arithos Designs; Mahesh U. Patil , CDAC Hyderabad; C.P. Ravikumar , Texas Instruments India; Vinod Geo Thomas , Cranes Software
35	DIGITAL CIRCUITS TEST AND DFT – Hyderabad August 11-14, 2008	Dr. Nilanjan Mukherjee , Prof. Sudhakar M. Reddy , Iowa University, and Dr. C.P. Ravikumar , TI India
34	12th IEEE VLSI Design And Test Symposium – VDAT2008 July 23-26, 2008 – Wipro Campus, Bangalore	
33	Design For Manufacturability And Reliability – Bangalore July 7, 2008	Prof. Sandip Kundu , University of Massachusetts, Amherst
32	Three-day Workshop on Audio Codecs and Data Converters June 16-18, 2008, Jadavpur University	K. Radhakrishna Rao , Supriyo Palit , Sandeep S.K. , Anand K. , Poornima Mohanachandran , Gaurav Jain , and Uttam Agarwal (Texas Instruments India); Vinod Geo Thomas (Cranes Software International); Gurjit Singh Gill (Gill Instruments); and Debnarayan Kar (Tata Consulting Services)
31	4th Workshop on Design Verification Methodologies DVM2008, April 25-26, 2008 - Bangalore	Prabhat Agarwal , Sankalp Semiconductor, Aniruddha Baljekar , NXP Semiconductors, Ansuman Banerjee , Interra Systems India, Gurudutt Bansal , Cadence Design Systems, Vishal Choudhary , NXP Semiconductors, Pallab Dasgupta , IIT Kharagpur, Kaushik De , Synopsys India, Sainath Karlapalem , NXP Semiconductors, Raj Mitra , Texas Instruments, Abhijit Ray , Cadence Design Systems, Badri Seshadri , NXP Semiconductors, Pradip Thaker , Analog Devices Inc., Srinivasan Venkataramanan , Synopsys India, Haridas Vilakathra , NXP Semiconductors
30	21st International Conference on VLSI Design And 7th Intl Conference on Embedded Systems January 4-8, 2008 HICC, Hyderabad, India	



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	2007	SPEAKERS / INSTRUCTORS
29	INTERCONNECT DESIGN AND VARIABILITY – IDV2007 December 13-14, 2007 – Bangalore (Includes proceedings of IDV Workshop 2006)	Juan C. Rey , Mentor Graphics Corporation; Kazuya Masu , Tokyo Institute of Technology; Ersed Ackasu , OEA International, Inc.; Noel Menezes , Intel Corporation; Sachin Sapatnekar , University of Minnesota; Tom Williams , Synopsys; Vish Sundararaman , Texas Instruments Inc., Dallas; Steffen Rochel , Blaze DFM Inc.; Nishath Verghese and Atul Sharan , Cadence Design Systems; Nagaraj, N.S. , Texas Instruments Inc., Dallas, Palkesh Jain and Gautam Kapila , Texas Instruments India; Madhav P. Desai , IIT Bombay, and Vani Prasad , Freescale Semiconductor; Vidyasagar Ganesan , AMD
28	DIGITAL CIRCUITS TEST AND DFT – Noida, UP August 13-17, 2007	Dr. Nilanjan Mukherjee , Prof. Sudhakar M. Reddy , Iowa University, and Dr. C.P. Ravikumar , TI India
27	11th IEEE VLSI Design And Test Symposium – VDAT2007 August 8-11, 2007 – Kolkata	
26	LOW-POWER DESIGN AND TEST - HYDERABAD JULY 30-31, 2007	Dr. Vishwani D. Agrawal , Auburn University and Dr. Shrivaths Ravi , Texas Instruments India
25	DESIGN FOR MANUFACTURABILITY AND RELIABILITY JULY 27, 2007 - KOLKATA	Prof. Sandip Kundu , University of Massachusetts, USA
24	DIGITAL VLSI DESIGN - IISc, BANGALORE July 23-27, 2007,	David Money Harris , Harvey Mudg College of Engineering, CA, USA and Prof. Bharadwaj Amrutur , IISc, Bangalore
23	2nd MIXED-SIGNAL VLSI DESIGN AND TEST – COIMBATORE APRIL 25-26, 2007	Dr. P.V. Anand Mohan , ECIL; Dr Shanthi Pavan , IIT Madras; Dr. Chetan D. Parikh , DA-IICT, Gandhinagar; Dr. M.C. Bhuvanewari , PSG College of Technology; Dr. R. Neelaveni , PSG College of Technology; Jais Abraham , InnoDes Solutions Pvt Ltd; Jairam Sukumar , Texas Instruments India; Asif Ahmad , Analog Devices; Sharat Chandra , Texas Instruments India; Arjun Prakash , Tessolve Services Pvt Ltd; Sheetal Morajkar , Texas Instruments India Pvt Ltd; Girish Vaidya , Wipro Technologies

22	3rd DESIGN VERIFICATION METHODOLOGIES - I²IT, PUNE April 5-6, 2007	Dr. P.P.Chakrabarti - IIT Kharagpur; Tarun Garg , Cadence Design Systems; Shanthamoorthi Velusamy , Wipro Technologies; Haridas V. , SoC Design Technology, NXP Semiconductors India; Dr.Kaushik De , Verification Business Unit, Synopsys India; Desingh D Balasubramanian , Poseidon-Systems India; Dr. Supratik Chakraborty - IIT Bombay; Aditya Kher , Synopsys India; Manikandan Panchapakesan , NXP Semiconductors India; Vishwanath B and Ankush Jain , NXP Semiconductors India; Bhaskar Karmakar , Texas Instruments India and Mrinal Das , Sankalp Semiconductor
21	4th VTU-VSI-ISA Confluence - BANGALORE (VLSI Design archive of all 4 meetings)	Visit for details of all presentations: http://vlsi-india.org/vsi/pub/confluence_24feb06.shtml
20	ESLD WORKSHOP 2007 – BANGALORE January 11-12, 2007	Prof. Nikil Dutt , Center for Embedded Computer System, UC Irvine; Dr. Rishiyur Nikhil , CTO, Bluespec Inc.; Charlie Hauck , VP Technologies, Bluespec Inc.; Brian Bailey , Brian Bailey Consulting, USA; Dr. Sachin Ghanekar , Tensilica; Aravinda Thimmapuram , NXP Semiconductors; Dr. Kanishka Lahiri , NEC-Labs; Dr. Sandeep Shukla , The Virginia Polytechnic and State University; Desingh Balasubramanian , Poseidon and Syed Saif Abrar , NXP Semiconductor; Srinivasan Venkataraman and Amit Sharma , Synopsys; T.S. Rajesh Kumar , Texas Instruments Bangalore
19	20th International Conference on VLSI Design And 6th Intl Conference on Embedded Systems January 6-11, 2007, Bangalore	
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	2006	SPEAKERS / INSTRUCTORS
18	INTERCONNECT DESIGN AND VARIABILITY – BANGALORE December 28-29, 2006	Dr. Jaijeet Roychowdhury , University of Minnesota, USA; Dr. Krishna Saraswat , Stanford University, USA; Dr. Ram Achar , Carleton University, Canada; Dr. Shankar Balachandran , IIT Madras, Chennai, India; Vijay Sindagi , Texas Instruments, India; Dr. Tejas Jhaveri , Carnegie Mellon University, USA; Dr. Dipu Pramanik , Synopsys, USA; Dr. Mustafa Celik , Dr. Kevin J Le , Extreme DA, USA; Dr. Sarma Vrudhula , Arizona State Univeristy, USA; Dr. Vivek De , Intel, USA
17	DFT FOR DIGITAL DESIGN – HYDERABAD September 4th – 6th 2006	C.P. Ravikumar , Senior Technologist, Texas Instruments, India, Jais Abraham , Head-Technology, InnoDes Solutions Pvt. Ltd.
16	DIGITAL CIRCUITS TEST AND DFT – BANGALORE August 17-19, 2006	Dr. Nilanjan Mukherjee , Prof. Sudhakar M. Reddy , Iowa University, and Dr. C.P. Ravikumar , TI India
15	10th IEEE VLSI Design And Test Symposium – VDAT2006 August 9-12, 2006 – Goa	
14	CIRCUIT MARGINALITIES – KOLKATA August 1, 2006	Prof. Sandip Kundu , University of Massachusetts, USA
13	DFT - THEORY AND PRACTICE - HYDERABAD July 27 – 29, 2006	Prof. Adit Singh and Prof. Vishwani Agrawal , Auburn University
12	DESIGN VERIFICATION METHODOLOGIES – PUNE March 24-25, 2006	A. Vasudevan , Wipro Technologies -Bangalore, Raj Mitra , Texas Instruments-Bangalore, Muralidhar Bolisetty , Synopsys-Bangalore, Venkatesan Swaminathan , Intel-Bangalore, Ms. Deepali Maydeo , Tensilica-Pune, Dr Shankar Balachandran , IIT Madras, Subir K Roy , Texas Instruments-Bangalore, Shailesh Dave , eInfochips Ltd-Pune, Vinaya Singh , Cadence Design Systems-Noida , Mahesha Puttanna and Sunil Vishwanathan , Wipro Technologies and Amit Sharma , Synopsys-Bangalore

11	ESLD WORKSHOP 2006 – BANGALORE January 9-10, 2006	<p> Prof. Arvind, Massachusetts Institute of Technology, USA; Brian Bailey, Brian Bailey Consulting, USA; Prof. Rajesh Gupta, University of San Diego, California, USA; Dr. Rishiyur Nikhil, CTO, Bluespec Inc.; Dr. Shiv Tasker, CEO, Bluespec Inc.; Mr. Sarang Shelke, Director Technology, Poseidon Systems, Bangalore; Mr. Bill Salefski, VP Technology, Poseidon Systems, California; Mr. Viswanath Chakrala, Specialist VLSI System Design, Wipro Technologies, Bangalore Mr. B.P.Srinivas, Senior Applications Engineer, Coware, Noida; Mr. Himanshu Sanghvi, Project Manager, Tensilica, California; Mr Nagendra Gulur Dwarakanath, Texas Instruments, India; Mr Badri Gopalan, Ageia, Bangalore; Mr Srinivasan Venkataraman, Synopsys, India; Mr Raghu Tupuri, General Manager (Silicon Design), Advance Micro Devices, Bangalore </p>
10	19th International Conference on VLSI Design And 5th Intl Conference on Embedded Systems January 3-7, 2006, Hyderabad	
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	2005	SPEAKERS / INSTRUCTORS
9	VLSI PHYSICAL DESIGN AUTOMATION – BANGALORE December 19-21, 2005	Dr.Dinesh Bhatia, University of Texas, Dallas
8	VLSI SIGNAL INTEGRITY – BANGALORE December 16 - 17, 2005	Dr. Ram Achar, Carleton University, Canada, Dr. Ashok Balivada, Analog Devices, India, Dr. Shabbir Batterywala, Synopsys, India, Arvind, Texas Instruments India and Dr. C.P. Ravikumar, Texas Instruments India
7	DFT COURSE – NEW DELHI December 15 - 17, 2005	Dr.Vishwani D. Agrawal, Auburn University and Dr.C.P. Ravikumar, Texas Instruments India
6	DESIGN VERIFICATION METHODOLOGIES – BANGALORE November 25, 2005	Mahesha Puttanna, Wipro Technologies, Srinivasan Venkataramanan, Synopsys, India, Badri Gopalan, Ageia Technologies, Venkatesan Swaminathan, Intel, Bangalore, Vinaya Singh, Cadence Design Systems, Sundaresan Kumbakonam, Broadcom, and Venkatesh Natarajan, Texas Instruments India
5	9th IEEE VLSI Design And Test Symposium – VDAT2005 August 10-13, 2005 – Mysore	
4	DFT "THEORY AND PRACTICE" – BANGALORE July 27-30, 2005	Dr.Vishwani D.Agrawal and Prof.Adit D.Singh (Auburn University)
3	LOW-POWER DESIGN TECHNIQUES – BANGALORE February 25-26, 2005	Dr. Bharadwaj Amruthur, IISc., Bangalore; Dr. V. Visvanathan, Texas Instruments, India; Dr. V. Ramgopal Rao, IIT Bombay, India; Dr Navakanta Bhat, IISc., Bangalore; Chandrashekhara Kypa and Christoph Heer, Infineon Technologies; Dr. K.Itoh, Hitachi, Japan; Dr. Y.N. Srikant, IISc., Bangalore; Dr. Christian Piguet, CSEM, Switzerland and Dr.C.P.Ravikumar, Texas Instruments India
2	RECENT ADVANCES IN MEMORY TECHNOLOGIES – BANGALORE January 10-11, 2005	Sreedhar Natarajan, MoSys Incorporated, Ottawa, CANADA; Dr.Nilanjan Mukherjee, Mentor Graphics, USA; Jayanta Lahiri, Alliance Semiconductors, Bangalore and Dr.C.P.Ravikumar, Texas Instruments India

1	18th International Conference on VLSI Design And 4th Intl Conference on Embedded Systems January 3-7, 2005, Kolkata	
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8	ESLD WORKSHOP 2006 - BANGALORE		250.00		
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14	INTERCONNECT DESIGN AND VARIABILITY - BANGALORE		250.00		
	2007				
15	ESLD WORKSHOP 2007 - BANGALORE		250.00		
16	4 th VTU-VSI-ISA Confluence (VLSI Design archive of all 4 meetings)		250.00		
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20	DESIGN FOR MANUFACTURABILITY AND RELIABILITY - KOLKATA		150.00		
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22	2 nd DCT-DFT COURSE - NOIDA		250.00	450.00	
23.	INTERCONNECT DESIGN AND VARIABILITY – BANGALORE		250.00	(Incl. IDV2006)	

	2008				
24.	4 th DESIGN VERIFICATION METHODOLOGIES – BANGALORE		250.00	(Incl. Past DVM Workshops)	
25.	AUDIO CODECS AND DATA CONVERTERS – JADAVPUR UNIVERSITY		250.00		
26.	DESIGN FOR MANUFACTURABILITY AND RELIABILITY - BANGALORE		150.00		



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5	VLSI DESIGN AND TEST WORKSHOPS 2002 - BANGALORE		250.00		750.00
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7	VLSI DESIGN AND TEST WORKSHOPS 2004 - MYSORE		250.00		750.00
8	VLSI DESIGN AND TEST SYMPOSIUM 2005 - BANGALORE		250.00		750.00
9	VLSI DESIGN AND TEST SYMPOSIUM 2005 (TUTORIALS-1) Analog Design and Synthesis Issues for Scaling CMOS Technologies Dinesh Sharma, IIT Bombay, Chetan Parikh, DA-IICT, and Ranga Vemuri, University of Cincinnati		150.00		
10	VLSI DESIGN AND TEST SYMPOSIUM 2005 (TUTORIALS-2) Implementation Challenges in Embedded Systems Ajit Rao, TI India; Mani Manoharan, Wipro; Indrajith Radhakrishnan, Wipro; Sadashivan Manickam, Wipro; Pradeep Ganesh Natarajan, Wipro		150.00		
11	VLSI DESIGN AND TEST SYMPOSIUM 2006 - GOA		250.00		750.00
12	VLSI DESIGN AND TEST SYMPOSIUM 2006 (TUTORIALS-1) Analog Design Prof. K.R.K. Rao, Texas Instruments, India, and Prof. Dinesh Sharma, IIT Bombay		150.00		
13	VLSI DESIGN AND TEST SYMPOSIUM 2006 (TUTORIALS-2) Low-power Electronics and Future Technologies Prof. Vishwani Agrawal, Auburn University; D. Mukhopadhyay and P.K. Basu, Jadavpur University; Venkatesh C, Indian Institute of Science, Bangalore		150.00		
14	VLSI DESIGN AND TEST SYMPOSIUM 2006 (TUTORIALS-3) Testing and Verification Baijayanta Ray, P.K. Venkataraghavan and S. Balasubramanian, Synopsys; Indranil Sengupta, IIT Kharagpur		150.00		
15	VLSI DESIGN AND TEST SYMPOSIUM 2007 - KOLKATA		400.00		750.00

16	<p>VLSI DESIGN AND TEST SYMPOSIUM 2007 Tutorials T1: ANALOG DESIGN AND BIOCHIPS Tutorial-1: Low Power Design Technique in Analog And Mixed-Signal Design Dr. Chetan Parikh (DAIICT) and Dr. Krishnapura (IIT Madras) Tutorial-2: Design And Test of Microfluidic Biochips Dr. K. Chakrabarty (Duke University, USA) T2: SYSTEM-ON-CHIP TEST Tutorial-3: Manufacturing Test Solutions for System-On-Chip Integrated Circuits Dr. E. Larsson (Linkoping University, Sweden) and Dr. K. Chakrabarty (Duke University, USA) Tutorial-4: Compression, Delay Test and Diagnosis: Ensure High Quality, Low Cost and Quick Yield Ramp of Nanometer Ics Navneet Kaushik, Shaleen Babu and Sameer Chillarige (Cadence) T3: POWER MANAGEMENT Tutorial-5: Power Management Circuits Design & Applications Amit Patra and S. Mukhopadhyay, IIT Kharagpur, Ram Anant, Biranchinath Sahu and S. Venkatraman, TI India</p>		250.00		
17	<p>VLSI DESIGN AND TEST SYMPOSIUM 2008 - Bangalore</p>		250.00		1000.00
18	<p>VLSI DESIGN AND TEST SYMPOSIUM 2008 T1: RF DESIGN AND TEST RFIC Design and Testing for Wireless Communications Vishwani Agrawal and Foster Dai (Auburn University) T2: LOW-POWER DESIGN Part-1: SoC Power Management Architecture Design and Verification Bhanu Kapoor, Mimasac; Shankar Hemmady, Synopsys; and Sandeep Aggarwal, TI India Part-2: Ultra Low-Power Processors for Embedded Systems Atul Lele (Texas Instruments) and Gurjit Singh Gill (Gill Instruments) T3: DESIGN VERIFICATION Part-1: Holistic Verification: Myth or The Magic Bullet? Pradip Thaker, Analog Devices Part-2: Foundations of Design Verification- Formal and Functional Approaches Anuman Banerjee; Kausik Datta; and Amit Roy (Interra Systems India Pvt. Ltd.) Part-3: Static Rule Checking and Cross-domain crossing Kaushik De, Synopsys</p>		250.00		
19	<p>VLSI DESIGN AND TEST SYMPOSIUM 2009 - Bangalore</p>		250.00		
20	<p>VLSI DESIGN AND TEST SYMPOSIUM 2009 Tutorials Tutorial – I: Open Source Embedded System Development using Beagleboard Syed Khasim (Texas Instruments India) Tutorial – II: Compact Modeling and PDK's Madabusi Govindarajan, Tamilmani Ethirajan, Abhisek Dixit, and Josef Watts (IBM) Tutorial – III Part 1: Test Cost Reduction Techniques, Current Practices, Challenges and Impact Sarveswara Tammali (Texas Instruments India) Part-2: Test Power Reduction Techniques: Current Practices, Challenges and Impact C.P. Ravikumar and V.R. Devanathan (Texas Instruments) Tutorial – IV Part-1: Telemedicine Poornima Mohanachandran (i2iTeleSolutions) Part-2: Assistive Devices for the Visually Impaired M Balakrishnan (IIT Delhi)</p>		250.00		

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