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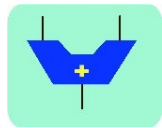
Third Design Verification Methodologies Workshop

April 5-6, 2007

I Square IT (I2IT) Pune Campus

P-14, Rajiv Gandhi Infotech Park, Hinjewadi, Pune 411057 Maharashtra

Organized by VLSI Society of India and International Institute of Information Technology, Pune



VLSI Society of India
<http://vlsi-india.org/vsi/>



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I2IT Pune
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Nanotechnologies have ushered in System-On-Chip designs with 50 million gates. Functional and timing verification of such designs is a formidable task. Design Verification has been known to be biggest contributor to the design cycle time. Statistics also indicate that design respins are often due to functional bugs detected late. Cutting down the time for verification is one of the major goals of design teams across the globe. Many new methodologies have emerged towards solving this problem. This two-day workshop is intended as a forum to discuss the new trends and methodologies for Design Verification. It is also a forum to share current practices in Design Verification.

HISTORY:

The first workshop in this series was held on November 25, 2005 at Hotel Atria, Bangalore and was attended by about 60 professionals. The details of the previous workshop can be found at:

http://vlsi-india.org/vsi/activities/dvw05_blr/

The second workshop was held during March 24-25, 2006 at Wipro Technologies, Pune and was attended by about 60 professionals. The details of the previous workshop can be found at:

http://vlsi-india.org/vsi/activities/dvm06_pne/

The workshop is suitable for practitioners of Design Verification and for students/faculty who are engaged in VLSI design projects.

Venue

[International Institute of Information Technology](http://www.isquareit.ac.in) (I²IT)

Microelectronics and VLSI, I2IT, Pune

P-14, Rajiv Gandhi Infotech Park, Hinjewadi

Pune 411057, Maharashtra

Phone: 020-22933441 FAX: 020-22934191

Access Details: <http://www.isquareit.ac.in/reachus.htm> ... [PDF](#)

Speakers

Dr. P.P.Chakrabarti - IIT Kharagpur

Tarun Garg, Cadence Design Systems

Shanthamoorthi Velusamy, Wipro Technologies

Bhaskar Karmakar, Texas Instruments India

Dr.Kaushik De, Verification Business Unit, Synopsys India

Desingh D Balasubramanian, Poseidon-Systems India

Tiju Jacob, Intel Corporation

Dr. Supratik Chakraborty - IIT Bombay

Haridas Vilakathra, SoC Design Technology, NXP Semiconductors India

Manikandan Panchapakesan, NXP Semiconductors India

Vishwanath B and **Ankush Jain**, NXP Semiconductors India

Aditya Kher, Synopsys India

Mrinal Das, Sankalp Semiconductor

For accommodation, please contact: **Mr.Harish**, I2IT Pune (harishm@isquareit.ac.in) Phone: 09890834503 updated

For registration, please contact: **Mr.Praveen**, I2IT Pune (praveench@isquareit.ac.in) Phone: 09860676053

Mr. Vamsi Krishna, I2IT Pune (npvamsi@isquareit.ac.in)

Program Committee

Dr. C.P. Ravikumar, Texas Instruments, India

Prof. Sheetal U. Bhandari, I2IT Pune

Local Organizing Committee

Prof. Sheetal U. Bhandari, I2IT Pune

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Mr. Santhosh Jagtap, Wipro Technologies, Pune

Mr. Harish, I2IT Pune (Accommodation)

Mr. Praveen, I2IT Pune (Registration)

Mr. Vamsi Krishna, I2IT Pune

Registration: Refer registration form

	Before March 15, 2007	After March 15, 2007
Professionals (Non-Members)	Rs. 4,000/-	Rs. 4,500/-
Professionals (VSI/ IEEE members)	Rs. 3,000/-	Rs. 3,500/-
Students/ Faculty (Non-members)	Rs. 2,500/-	Rs. 3,000/-
Students/ Faculty (VSI/ IEEE members)	Rs. 2,000/-	Rs. 2,500/-

Please also register using the online registration form at <http://vlsi-india.org/vsi/activities/reg.shtml> apart from sending the filled hardcopy of registration form, and to notify spot-registration.

Program Schedule

... April 5 – Thursday ...

08.00 – 09:00 AM	Registration
09:00 – 09.30 AM	Inauguration
09.30 – 10.30 AM	Session I Keynote Talk – Static Checker Technology: How it can help in Design Verification Dr.Kaushik De, Verification Business Unit, Synopsys India
10.30 – 11.00 AM	Tea
11.00 – 12.00 PM	Session II Formal Protocol verification using Assertion IPs Tarun Garg, Cadence Design Systems
12:00 – 12.30 PM	Session III SystemVerilog and SystemC for an Effective Design and Verification Shanthamoorthi Velusamy, Wipro Technologies
12.30 – 01:00 PM	Session IV System Level Analysis and Verification: An Industry Perspective Bhaskar Karmakar, Texas Instruments India
01.00 – 02.00 PM	Lunch
02.00 – 03.00 PM	Session V Keynote Talk – Challenges in Formal Methods for Intent Specification and Verification Dr. P.P.Chakrabarti – IIT Kharagpur
03.00 – 03.30 PM	Tea
03.30 – 04.30 PM	Session VI Tutorial - An Expedition to The System Modeling World Desingh D Balasubramanian, Poseidon-Systems India
04.30 – 05.30 PM	Session VII Verification of the 80 core, 1.28 Teraflop Network-on-Chip in 65nm CMOS Tiju Jacob, Intel India
End of Day-1	

... April 6 – Friday ...

08.30 – 09:30 AM	Registration
09.30 – 10.30 AM	Session I: Keynote Talk – Battling State Space Explosion: The Road Traveled and The Road Ahead Dr. Supratik Chakraborty – IIT Bombay
10.30 – 11.00 AM	Tea
11.00 – 11.45 AM	Session II Reusable Debug Infrastructure in Multi-core SoC Haridas Vilakathra, SoC Design Technology, NXP Semiconductors India
11.45 – 12.15 PM	Session III Sub-System Design and Verification Methodology Manikandan Panchapakesan, NXP Semiconductors India
12:15 – 01.00 PM	Session IV Configurable IP! - Overcoming the Verification Challenges Vishwanath B and Ankush Jain, NXP Semiconductors India
01.00 – 02.00 PM	Lunch
02.00 – 03.00 PM	Session V SystemVerilog based Verification using VMM: An Overview Aditya Kher, Synopsys India
03.00 – 03.30 PM	Tea
03.30 – 04.30 PM	Session VI Challenge in Mixed-Signal/Analog Verifications , Roads Ahead Mrinal Das, Sankalp Semiconductor, India
04.30 – 5.30 PM	Panel Discussion Details TBD
End of Workshop	

Speakers brief-bio and abstract:

DAY - 1

Static Checker Technology: How it can help in Design Verification

Dr. Kaushik De received B. Tech from IIT Kharagpur, and MS and PhD from University of Illinois at Urbana-Champaign. He worked in various technical & management roles in LSI Logic, Ambit, Cadence, Synopsys, and various startup companies, in US and India. He has worked in the area of Synthesis, DFT, and Design Verification. Currently he is working in Design Verification area, driving the static checker technology at Synopsys. He has published more than 20 technical papers at conferences and journals, and holds 5 US patents.

Abstract: As design complexities are growing, design verification problem is exploding. Simulation remains the main vehicle for design verification. However, design complexities make it extremely difficult to cover all cases of the design. Formal verification are used to prove properties of the design, however the capacity of the tool remains an obstacle. In addition, Formal verification technology usage requires deep expertise. Static Checker technology offers another very good alternative, which can identify potential issues in the design by doing static analysis of the design. For example, it can identify if the design can have simulation synthesis mismatch or potential race condition during simulation, or operand type or width mismatch, unintentional latch in the design, etc. In addition, it can detect many fundamental issues such as clock/reset/connectivity, etc.

The modern designs have many clock domains, and special care need to be taken in designing the part where signal traverses from one clock domain to another. Static checker can identify issues with respect to clock domain crossing of the signals. It can also detect correctness in signal connectivity in multi-power domain designs. Hence, deployment of static checker technology will greatly enhance the design verification capability.

Formal Protocol verification using Assertion IPs

Tarun Garg is senior member of technical staff at Cadence Noida R&D facility. He has over 6 years of experience in EDA product design and development in the area of formal assertion based verification. He has also done extensive work in handling PSL and SVA in formal verification. Tarun holds a bachelor's degree in electronics and communications from Delhi Institute of Technology, Delhi.

Abstract: With design reuse, the importance of standard protocols (e.g. OCP, AXI etc.) is increasing. This creates a need a reusable verification technique and methodology. This presentation discusses how assertion IPs in conjunction with formal analysis can be used to do protocol compliance checks in a reusable environment. Presentation also gives an overview of one of the standard protocols.

SystemVerilog and SystemC for an Effective Design and Verification

Shanthamoorthi Velusamy is Senior Verification/System Modeling Consultant at Wipro technologies with over 9 years of experience in ASIC Verification and System Modeling. He has architected Verification Environments using languages like Verilog, VHDL, Vera, C/C++ and SystemC for Networking, Computing and Storage domain chips. He has earned his BE in Electronics and Communication from IRT Tech, Erode and MS in Microelectronics from BITS, Pilani.

Abstract: With the complexity of ASIC and SoC designs spiraling out of control, Chip Design and Verification are becoming more of Object Oriented. The utilization of C and C++ for specific aspects of the design flow, such as creating a golden reference model for the design, test bench and test cases development, is becoming imperative. New technologies and tools have arrived which addresses many of the problems of interfacing C/C++ to HDL. SystemC has the capabilities to cross the boundary of the two design languages, and together with Simulator's native integration, SystemC can be used seamlessly with HDL Languages.

The key to success in ASIC and SoC design is to choose and use the language that offers the most effective abstraction level for the task at hand with more reusability. This presentation gives some insight into this as how SystemVerilog and SystemC can be used for an effective Design and Verification.

System Level Analysis and Verification: An Industry Perspective

Bhaskar Karmakar received the B.Tech. Degree in Electrical Engineering from the Indian Institute of Technology, Kharagpur, India, in 1995. He has over 11 years of industry experience in EDA and semiconductor companies worldwide.

He is currently Member, Group Technical Staff in Texas Instruments, Bangalore, India, where he leads several projects related to the research and development of design tools and methodologies for front-end design, front-end and system-level verification, and quality and predictability in SoC design.

Mr. Karmakar has published in international and internal conferences and has been nominated for best paper awards. He regularly reviews papers for leading conferences. His research interests include RTL synthesis, HDL simulation, and SoC performance analysis and verification.

Abstract: As recent experiences have shown, some SoCs fail to meet performance specifications, and these failures are identified very late in the design cycle - where the only feasible mitigation (if at all possible) is a firmware work around. The root cause of most performance failures can be traced back to insufficient architectural analysis and system-level verification. It follows then, that system-level verification is still an open problem in the industrial context.

This talk first describes the current methods used by architects and designers to perform system-level analysis and verification on industrial SoC designs, and the inherent limitations of such methods. Next, it identifies the principal requirements, which any system level modeling and analysis methodology must meet, and highlights few technologies, which need to be developed, before such methodologies can gain mainstream acceptance. Finally, future extensions and applications of system-level analysis and verification techniques are also discussed.

Challenges in Formal Methods for Intent Specification and Verification

Dr. Partha P Chakrabarti, completed his BTech in 1985 and PhD in 1988 from the Dept of Computer Science & Engg, Indian Institute of Technology Kharagpur. He joined the same department as a faculty member in 1988 and is currently a Professor. He was the Professor-in-Charge of the state of the art VLSI Design Laboratory which he set up and is currently the Dean of Sponsored Research and Industrial Consultancy at IIT Kharagpur. His areas of interest include Artificial Intelligence (AI), CAD for VLSI & Embedded Systems and Algorithm Design. Dr Chakrabarti has

made important contributions in the area of CAD for VLSI, especially in the areas of high level and logic synthesis and formal verification. Many of the AI methods developed by him and his group have been applied to real-life VLSI design problems in industry and have been incorporated in industry level tools. He has published more than 170 papers and has been awarded many prizes including the President of India Gold Medal, Young Scientist Fellowships from INSA and INAE, Swarnajayanti Fellowship and the Shanti Swarup Bhatnagar Award. He is a fellow of INSA, IASc and INAE.

Abstract: Every design process begins with the creation of the first set of formal specifications and the first behavioural design or "golden model". These form the basis of all subsequent design transformation steps, namely design refinement, synthesis and optimization. With the growth of design complexity, new formal approaches are required for automation and assistance of even this first step in the design process. This talk will provide a glimpse of the techniques that are being used, including recent approaches to grapple with the issues of increasing design complexity and discuss open problems that continue to challenge us.

Tutorial - Transaction Level Modeling

Desingh D Balasubramanian is currently a Senior Member Technical Staff in the system level simulation and modeling team of Poseidon Design Systems. His areas of interest include computer architecture, Media processor architectures, system level modeling for design space exploration and design methods for efficient HW/SW co-design. He is a post-graduate degree (MTD) in Embedded Systems from National University of Singapore & Technical University of Eindhoven. He received his B.Tech in Electronics from Madras Institute of Technology, Chennai.

Abstract: The goal of this expedition is to enable the SoC design community get a quick technical overview on the latest trends in Transaction Level system modeling. This tutorial addresses the following topics

1. Use Case scenarios in TLM based design flow and typical requirements for a TL platform for various use cases
2. Need for Modeling standards for inter-operability and the necessary model interface standards to achieve inter-operability
3. Upcoming standards such as TLM 2.0 and SPIRIT and available tools for the design community

Verification of the 80 core, 1.28 Teraflop Network-on-Chip in 65nm CMOS

Tiju Jacob received B. Tech degree in Electronics and Communication Engineering from NIT, Calicut in 2000 and M. Tech degree in Microelectronics and VLSI design from IIT Madras in 2003. He joined Intel Corporation, Bangalore in 2003 and currently a member of Circuit Research Labs. His areas of interests include low power high performance circuits, many core processors and advanced prototyping.

Abstract: The ever-shrinking size of CMOS transistor brings the promise of scalable network-on-chip architecture (NoC) containing hundreds of integrated processing elements with on-chip communication. This NoC contains 80 tiles arranged as 10x8 2D array of floating point cores and packet switched routers operating at 4GHz. The 65nm, 100M transistor chip has a performance of 1 Teraflop at 1V while dissipating just 62 watts. The design employs mesochronous clocking, fine-grained clock gating and dynamic sleep transistor techniques to achieve the highest energy efficiency. While these techniques augmented the verification complexity, the tiled design approach and modular design methodology reduced the top-level verification effort. This presentation discusses the various verification techniques used during the logic, circuit and physical design of the Terflop chip.

DAY - 2

Battling State Space Explosion: The Road Traveled and The Road Ahead

Dr. Supratik Chakraborty is an Associate Professor of Computer Science and Engineering at IIT Bombay, where he has been since 1999. From 1998 to 1999, he was a member of the research staff of the Advanced CAD Research group at Fujitsu Laboratories of America, Inc, where he worked on timing optimization of high-speed circuits by logical transformations. He received his B. Tech. in Computer Science and Engineering from IIT Kharagpur in 1993, and was awarded the President of India Gold Medal. Subsequently, he received his M.S. and Ph.D. degrees in Electrical Engineering from Stanford University in 1995 and 1998.

His research interests include design, analysis and verification of asynchronous and mixed synchronous-asynchronous systems, and formal verification of hardware and software systems, and he has several publications in these areas. He has been a Principal Investigator at the Centre for Formal Design and Verification of Software at IIT Bombay since 2000.

Abstract: State space explosion is a significant bottleneck in several formal verification (and other design, analysis and optimization) tasks that use reachability analysis as a core procedure. While sizes of designs have kept increasing in accordance with Moore's Law, it has become practically impossible for reachability analysis engines to keep pace due to the inherent computational complexity of the underlying problem. In this talk, we will discuss several approaches to address this problem, and outline future directions in this regard. We will discuss how practically useful reachability analyzers can be built for large designs by carefully striking a favourable balance between accuracy and efficiency, while guaranteeing that errors are always one-sided. We will also outline a framework being developed at IIT Bombay that allows a designer the flexibility to specify custom-made strategies for reachability analysis of different circuits, thereby allowing domain knowledge to be incorporated in the search strategy.

Reusable Debug Infrastructure in Multi-core SoC

Haridas Vilakathra started his career as a scientist at DRDO (1994-1998) where he was involved in the development of hardware and software for a flight control system for LCA and airborne sonar. He later worked for NEC Japan (1998 - 2000) on hardware IP development, system integration and verification for a W-CDMA base station. He is presently with NXP semiconductors (2001-current) where his responsibilities include architecting of reusable hardware IP cores and processor based sub system. He has published more than 15 papers in national and international forums. His current interest is in defining a multi processor video sub-system for consumer electronics applications and reusable debug infrastructure. HE is also involved in standardizing a digital serial interface for wireless modems between the digital modem and analog front end, including RF.

Abstract: With increase in hardware and software content in today's complex SoC, it becomes a necessity to verify such system from a system

viewpoint. Providing a means to effectively debug such systems from a system perspective is vital in help to pin point the problem and thereby reduce the number of chip re-spin. This paper outlines a system level reusable hardware-software debug infrastructure for a complex multi core SoC and describes how this can be integrated with existing third party debug tools such as ARM Multilce and logic analyzers. The concepts are illustrated through a project case study. This approach provides a "debug backplane" to address dense and complex multi-core systems analysis, such as processor behavior, embedded logic block functions and deeply embedded bus traffic.

Sub-System Design and Verification Methodology

Manikandan Panchapakshan, is a technical lead at NXP Semiconductors in the area of IP-level and subsystem-level verification. He is responsible for creation of test plan, unit-level verification, testing, and integration of IP. He is also responsible for testing of interconnectivity and interoperability of the su-systems.

Abstract: The system integration and verification has been a challenge in the semiconductor industry. Different methodologies and tools have evolved to address these challenges in various aspects. Nx-Builder is the SPIRIT (Structure for Packaging, Integrating and Re-using IP within Tool flows) based standard NXP design environment that addresses the SoC (System on Chip) design/integration challenges through extensive utilization of architecture ReUse, IP ReUse, verification software Reuse, hardware-software (HW-SW) co-verification, FPGA partition and design flow automation. Nx-Builder helps in correct-by-construction designs and allows rapid development of new systems.

This presentation is the introduction to the Nx-Builder based methodology and shows how it can be used to define, develop and verify a platform instance. This paper highlights the current methodology and features of Nx-Builder and illustrates how these differentiating design capabilities are being applied today to accelerate SoC development. Furthermore, the paper covers how Nx-Builder can be customized to cater for a wide range of platform architectures.

Configurable IP! Overcoming the Verification Challenges

Vishwanath B has over 3 years experience in the industry. He completed BE from Mumbai University, and obtained M.Tech from VNIT Nagpur. In his present job as a Senior Design Engineer at NXP Semiconductor India, he is involved with Design & verification in on-chip interconnect domain with interest in developing reusable & effective verification environment.

Ankush Jain completed his BE Electronics from PES college of Engineering. He has over 5 years industrial experience. In his present Job as a Technical Leader at NXP Semiconductor India, he is involved with Development of verification suite for different configurable IPs having interface like AHB, AXI, VPB, APB etc., using languages like e, TCL, Verilog and VHDL.

Abstract: The key concept in SoC design is that a chip can be constructed rapidly using third-party and internal IPs. In this context configurable IPs are need of the hour as it can be easily mapped to meet specific SoC requirements. Such IPs must provide a wide range of configurability so as to meet the requirements of different SoC applications, at the same time easy to specify and develop by the user. Configurable IPs with hundreds of parameters & complex design state space offers significant verification challenges to the IP provider.

This paper proposes a specman based verification methodology to verify highly configurable IPs. All the modules in specman environment including functional coverage, sequences & scoreboards are embedded in a scripting language to configure as per user requirement. A customized tool is then used to extract an automatically tailored verification environment for the selected configuration. The verification suite is developed in a modular fashion based on the eRM methodology wherein the advance techniques like assertion assisted structured scoreboards, orderly executed functional & performance patterns are used to simplify the verification of parametric designs.

SystemVerilog based Verification using VMM: An Overview

Aditya Kher is a Corporate Application Engineer at Synopsys. In this role he works on VCS Native Testbench and the Verification Methodology Manual (VMM) for SystemVerilog. Aditya joined Synopsys in 2004 and has around 5 years experience in the hardware and EDA industries. Previous to Synopsys, Aditya was employed at Tata Elxsi, where he held position as a Verification Engineer.

Abstract: VMM methodology helps both new and experienced verification engineers to accelerate the creation of robust, reusable verification environments. These verification environments have a layered testbench architecture that follow industry best practices for coverage-driven, constrained-random and assertion-based verification technique.

Challenge in Mixed-Signal/Analog Verifications, Roads Ahead

Mrinal Das brings in over 10 years of industry experience in VLSI, Mixed Signal IC Design and RF System on Chip (SOC) product development. Prior to Sankalp, Mrinal was the Manager for Bluetooth RF Product development in Texas Instruments India.

He joined Texas Instruments India in 1996 as an IC Design Engineer. He was part of the project team that delivered the first system on chip codec for voice band modems. In 1998, Mrinal was the project lead for a core team that started a major new activity in TI India - design of Digital Still Camera front End. After that he held various technical and leadership roles in Mixed Signal group and was instrumental to create solid foundations for Digital Still Camera (DSC) and Cable Modem team. Today both these teams create some of the strongest pillars, providing state of the art products from TI India.

In 2000, Mrinal was assigned a responsibility creating analog friendly process technology in digital deep sub-micron process nodes. His involvement continued while working together with TI Silicon Technology Development (SiTD) team for analog/RF specific-device needs.

From 2001 onwards Mrinal was deeply involved in RF SOC developments in different technical and Management roles. This involves the Digital Radio Processor development, Wireless LAN SOC and Bluetooth Enhanced Data Rate single chip solution.

In 2002, he was elected Member Group of Technical Staff (MGTS) in TI India for his technical contributions to TI's success.

Mrinal has 4 US patents granted, and more than 4 International IEEE publications. He was elected IEEE Senior Member in 2006, and also serves the IEEE Review Committee for VLSI Conference.

Mrinal has a Bachelor's Degree in Electronics and Communications Engineering from Jadavpur University in 1996. One of his many passions involves taking Mixed Signal semiconductor to different parts of India.

Abstract: Historically Digital verification methodology had been in existence for quite some time. This has allowed the digital chip development to be very systematic and hardly bugs lead up to the fabrication level. Analog verification mostly, is left with the expertise of the designers, which leads to unwanted errors to pass through. With the advent of ultra deep submicron technology and increasing mask cost, significance of smallest bug has gone high by many fold. Hence it's important for a Mixed Signal Design to be correct as far as connectivity, functionality and parametric goes right at the first time.

This talk talks about commonly used methodology for Mixed Signal verification with a special focus on block level verification and top-level verification. It also mentions some of the methodology driven automations that are being proposed to make a Analog design correct by construction, and without leaving it to chances of experience and lessons learnt.

Automation at every step is the only way to make complex analog chips to come to market faster and with higher efficiency. This talk will touch on automations that are implemented at the grass root level of Mixed Signal Verification.

