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VLSI Society of India

# Workshop on Verification Methodologies

November 25, 2005, Hotel Atria, Bangalore, India

In cooperation with



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Design Verification Forum - India, IEEE Circuits and Systems Society

Design Verification is one of the most time-consuming of all the steps in the design flow. Many new methodologies are emerging to improve the cycle time of design verification. This workshop will provide an exposure to some of the recent developments in VLSI Design Verification.

## Schedule

08.30 AM – 09.00 AM	Registration
09.00 AM – 09.15 AM	Inauguration Design Verification Forum – India: Mission and Campaign – Harish Y.S., Texas Instruments India
09.15 AM – 10.30 AM	Mahesha Puttanna, Wipro Technologies Getting to 100% Functional Coverage – Challenges for the Verification Engineer
10.30 AM – 11.00 AM	Tea Break
11.00 AM – 12.00 NN	Srinivasan Venkataramanan, Synopsys, India and Badri Gopalan, Ageia Technologies An Overview of System Verilog
12.00 NN – 01.00 PM	Venkatesan Swaminathan, Intel, Bangalore An Environment for executing full chip pre-silicon environment on Pos-silicon
01.00 PM – 02.00 PM	Lunch
02.00 PM – 03.00 PM	Vinaya Singh, Cadence Design Systems Is Formal ABV usable for real verification?
03.00 PM – 04.00 PM	Sundaresan Kumbakonam, Broadcom How HVL based environments are beneficial over Verilog/C based environments
04.00 PM – 04.30 PM	Tea Break
04.30 PM – 05.30 PM	Venkatesh Natarajan Emulation-based Verification
05.30 PM – 06.00 PM	Conclusions

## Speakers

Mahesha Puttanna	Mahesha Puttanna is verification lead and a consultant at Wipro technologies with 8 years of experience in ASIC Verification. He has been instrumental in developing verification methodology for complex ASICs that has consistently delivered first silicon success. He developed test benches using languages like Verilog, VHDL, Vera and Specman. Mahesha earned his M. Tech from Sri Jayachamarajendra college of engineering, Mysore.
Srinivasan Venkataramanan	Srinivasan Venkataramanan is a senior Verification Solutions engineer with Synopsys Bangalore with extensive experience in pre-silicon verification. His primary interests are in constrained random, coverage driven, and assertion based verification. He has co-authored two books on assertion based verification and has published several papers in different forums. He holds a Masters degree in VLSI Design from IIT Delhi. He has work experience at Intel and Philips in the areas of RTL design and Pre-Silicon Verification.
Badri Gopalan	Badri Gopalan has extensive experience working with HDLs and HVLs as a user, developer and architect. He currently works at Ageia Technologies. He has spent about 10 years at Synopsys, Riverstone Networks, and Cadence Design Systems. Badri has an MSEE from the University of Maryland, College Park and a B.Tech (EE) from IIT Bombay.
Venkatesan Swaminathan	Vekatesan Swaminathan has several years of industry experience in design verification, test generators for pre silicon and post silicon environments. His interests are in validation environments for today's networking and processor platforms and building pre silicon environments, which can be reused for post silicon testing. He has published papers in various forums like IPSOC.
Sundaresan Kumbakonam	Sun Kumbakonam has over 16 years of experience in the field of Design Verification. He has put together from scratch teams and DV environments that have helped take to production, very complex ASICs and SOC's in the domain areas of PA-RISC based servers, MPEG set-top boxes, Internet Security and Network Switching. He has hands on experience on various environments for DV, from home brewed Verilog/C-PLI based, to ones that used Specman and VERA. He contributed as a reviewer of the book, Design Verification with E, by Samir Palnitkar. Sun also has been a judge for the last two years in the DV track of SNUG. He currently heads the network switching design group in India, for Broadcom. He has a dual Master's degree from BITS Pilani.
Venkatesh Natarajan	Venkatesh Natarajan has a B.E (Electronics) degree from University Visvesvaraya College of Engineering, Bangalore (1991). After spending a year with CMC Ltd, he has been with Texas Instruments since 1992. He started his career in TI in the memory modeling group and later moved to the C27x and C28x CPU architecture and verification team. His areas of expertise and current focus are CPU and debug architectures (CPU emulation) and hardware emulation and prototyping techniques for SoC.
Vinaya Singh	Vinaya Singh is M.Tech in computer science from IIT Bombay and has over 10 years of experience in EDA product developments in the area of verification and synthesis. Vinaya is member of Accellera OVL committee and was task leader of IEEE VHDL synthesis standard 1076.6-2004. Vinaya holds two patents in the area of formal verification. Currently he is working as Senior Member of Consulting Staff at Cadence NOIDA R&D facility..
Harish Y.S	Harish Y.S. has an MS degree from BITS, Pilani, BE (Electronics & Comm)degree from BVBCET, Karnataka University (1998). His work experience includes 1 year at the Indian Institute of Science and six years with Texas Instruments, where he is involved in CPU design and verification. His area of focus is functional verification, methodologies for verification involving test generation, formal techniques and non-volatile memory testing.

## Course Fee

Before October 31, 2005		After October 31, 2005	
Professionals (Non- Members)	Rs. 1,500/-	Professionals (Non- Members)	Rs. 2,000/-
Professionals (VSI/ IEEE members)	Rs. 1,000/-	Professionals (VSI/ IEEE members)	Rs. 1,500/-
Students (Non-members)	Rs. 600/-	Students (Non-members)	Rs. 750/-
Students (Members of VSI/ IEEE)	Rs. 500/-	Students (Members of VSI/ IEEE)	Rs. 650/-

